REMARKS

In the non-final Office Action, the Examiner objects to claim 30 due to an informality; rejects claims 14-23 and 25-29 under 35 U.S.C. § 103(a) as unpatentable over LO et al. (U.S. Patent No. 6,324,178) in view of YOKOYAMA et al. (U.S. Patent No. 5,303,344), and further in view of STONER et al. (U.S. Patent No. 6,052,383); rejects claims 24 and 32-34 under 35 U.S.C. § 103(a) as unpatentable over LO et al. in view of YOKOYAMA et al., and further in view of STONER et al. and ALBAL et al. (U.S. Patent No. 4,821,265); rejects claim 30 under 35 U.S.C. § 103(a) as unpatentable over LO et al. in view of YOKOYAMA et al., and further in view of HIGUCHI et al. (U.S. Patent Application Publication No. 2003/0193965); and rejects claim 31 under 35 U.S.C. § 103(a) as unpatentable over LO et al. in view of YOKOYAMA et al., and further in view of HIGUCHI et al. and TSUCHIYA et al. Applicants respectfully traverse these rejections.

By the present amendment, Applicants amend claim 30 to improve form. Claims 14-34 remain pending.

Claim 30 stands objected due to an informality. Applicants amend claim 30 herewith to address the Examiner's concerns. Accordingly, withdrawal of the objection to claim 30 is respectfully requested.

Claims 14-23 and 25-29 stand rejected under 35 U.S.C. § 103(a) as unpatentable over LO et al. in view of YOKOYAMA et al., and further in view of STONER et al. Applicants respectfully traverse this rejection.

Independent claim 14 is directed to a packet processing apparatus for converting packet data through a plurality of layers. The apparatus includes a packet memory for storing at least a user information portion of the packet data; and a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception, used in a process of a higher layer processing portion for higher layer processing operations, and read by the lower layer processing portion at a time of the packet data transmission, wherein the lower layer processing portion reads the header portion from the shared memory. The lower layer processing portion and the higher layer processing portion access a same memory space of the shared memory through physically different memory buses. LO et al., YOKOYAMA et al., and STONER et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, LO et al., YOKOYAMA et al., and STONER et al. do not disclose or suggest a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception, used in a process of a higher layer processing portion for higher layer processing operations, and read by the lower layer processing portion at a time of the packet data transmission. The Examiner admits that LO et al. does not disclose a shared memory and relies on step 1034 of Fig. 13, and steps 1014-1016 of Fig. 12, of YOKOYAMA et al. for allegedly disclosing a shared memory that is written by a lower layer processing portion at a time of the packet data reception and read by the lower layer processing portion at a time of

the packet data transmission (Office Action, pg. 3). Applicants respectfully disagree with the Examiner's interpretation of YOKOYAMA.

Step 1034 in YOKOYAMA et al.'s Fig. 13 indicates that if the LLC header is the UI frame, and if the UI frame is normal, data transfer processor unit 100-3 generates a primitive to the network layer in the third entry E3 of the command descriptor 31 (col. 9, lines 59-62). YOKOYAMA et al. discloses that a primitive is a control signal (col. 4, lines 52-57). This step of YOKOYAMA in no way relates to a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception and read by the lower layer processing portion at a time of the packet data transmission, as required by claim 14.

Moreover, the Examiner relies on YOKOYAMA et al.'s element 30 as allegedly corresponding to the recited shared memory (Office Action, pg. 3). YOKOYAMA et al.'s element 30 corresponds to buffer memory 30. With this interpretation in mind, YOKOYAMA et al.'s step 1034 does not disclose or suggest storing a header portion of the packet data to buffer memory 30, which is written by a lower layer processing portion at a time of the packet data reception and read by the lower layer processing portion at a time of the packet data transmission, as would be required by the Examiner's interpretation of claim 14.

YOKOYAMA et al.'s Fig. 12 describes a transmission operation of the protocol processor (col. 3, lines 16-17). With respect to steps 1014-1016, YOKOYAMA et al. discloses data transfer processor unit 100-3 generating the LLC header in accordance with the contents of the third entry E3 of the command descriptor 31 read from the buffer

memory as in the network layer (steps 1014 and 1015) and after the command to the MAC control processor 50 is generated in the fourth entry E4 of the command descriptor 31, the CDID being supplied through the primitive path 22-4, thereby starting the MAC control processor 50 (step 1016). These steps of YOKOYAMA et al. do not disclose or suggest a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception and read by the lower layer processing portion at a time of the packet data transmission, as required by claim 14.

Even assuming, for the sake of argument, that the above steps of YOKOYAMA et al. could reasonably be construed to disclose a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception and read by the lower layer processing portion at a time of the packet data transmission, Applicants submit that one skilled in the art at the time of Applicants' invention would not have been motivated to incorporate this alleged teaching of YOKOYAMA et al. into the LO et al. system, absent impermissible hindsight. With respect to motivation, the Examiner alleges "it would have been obvious to one skilled in the art ... to have a shared memory in the apparatus of Lo in order to provide flexible protocol processor" and points to col. 1, lines 60-63, of YOKOYAMA et al. for support (Office Action, pg. 3). The Examiner's motivation is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation has consistently been held to be insufficient for establishing a *prima facie* case of obviousness. Moreover, the Examiner does not explain why incorporating a shared memory for storing a header

portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception and read by the lower layer processing portion at a time of the packet data transmission into the LO et al. system would result in a flexible protocol processor. Applicants submit that the Examiner's motivation is based on impermissible hindsight.

> Nevertheless, at col. 1, lines 60-63, YOKOYAMA et al. discloses:
>
> It is still another object of the invention to provide a communication protocol processor comprising a plurality of processors having excellent general-purpose applicability and flexibility.

Contrary to the Examiner's allegation, this section of YOKOYAMA et al. does not explain why incorporating a shared memory for storing a header portion of the packet data, which is written by a lower layer processing portion at a time of the packet data reception and read by the lower layer processing portion at a time of the packet data transmission into the LO et al. system would result in a flexible protocol processor. Instead, this section of YOKOYAMA et al. merely discloses a communication protocol processor comprising a plurality of processors.

The disclosure of STONER et al. does not remedy the above deficiencies in the disclosures of LO et al. and YOKOYAMA et al.

LO et al., YOKOYAMA et al., STONER et al. do not further disclose or suggest a lower layer processing portion and a higher layer processing portion accessing a same memory space of a shared memory through physically different memory buses, as also required by claim 14. The Examiner admits that LO et al. and YOKOYAMA et al. do not disclose this feature and relies on elements 9, 11, 13, and 15, in Fig. 1 of STONER et

al. for disclosing "separate component buses for pipeline processing" (Office Action, pp. 3-4). Applicants respectfully disagree with the Examiner's interpretation of STONER et al.

STONER et al.'s Fig. 1 depicts a switch module 1 that includes an ATM interface means 17, LAN interface means 19, and a packet memory 7 connected to a packet switching processor 21 and a management processor 23. In STONER et al.'s Fig. 1, elements 9, 11, 13, and 15 correspond to port means of packet memory means 7 that can separately read and write information from and to packet memory means 7 (col. 4, lines 11-14). STONER et al. does not disclose or suggest that one of these ports 9, 11, 13, and 15 can access a same memory space of packet memory means 7 through physically different memory buses, as required by claim 14. Also, Applicants submit that one skilled in the art would not construe ports 9, 11, 13, and 15, which is part of packet memory means 7, as corresponding to a lower layer processing portion and a higher layer processing portion.

Even assuming, for the sake of argument, that the above portion of STONER et al. could reasonably be construed to disclose a lower layer processing portion and a higher layer processing portion accessing a same memory space of a shared memory through physically different memory buses, Applicants submit that one skilled in the art at the time of Applicants' invention would not have been motivated to incorporate this alleged teaching of STONER et al. into the LO et al. system, absent impermissible hindsight. With respect to motivation, the Examiner alleges "it would have been obvious to one skilled in the art ... in order to give dedicated access between the components" and

points to col. 4, lines 11-14 and 43-54, of STONER et al. for support (Office Action, pg. 4). The Examiner's motivation is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation has consistently been held to be insufficient for establishing a *prima facie* case of obviousness. Applicants submit that the Examiner's motivation is based on impermissible hindsight.

Nevertheless, at col. 4, lines 11-14, STONER et al. discloses:

> The memory means 7 also includes a PSP port means 15 and a MCPU port means 13. Each of the port means 9, 11, 13 and 15 can separately read and write information from and to the memory means 7.

This section of STONER et al. does not explain why incorporating a lower layer processing portion and a higher layer processing portion accessing a same memory space of a shared memory through physically different memory buses into the LO et al. system would result in dedicated access to components. Instead, this section of STONER et al. merely discloses that memory means 7 include ports 9, 11, 13, and 15 that can separately read and write information from and to memory means 7.

At col. 4, lines 43-54, STONER et al. discloses:

> By having two separate and distinct ports on the memory 7, the writing of data by the ATM interface means 17 to the memory 7, does not effect any reading or writing of information from the LAN interface means 19 to the LAN connector and LAN packet channel bus. Likewise, the LAN interface means 19 writing to the memory 7 does not prevent the ATM interface means 17 from reading or writing to the ATM connector 3. The two separate and distinct ports on the memory 7 can thus allow a substantially simultaneous two way transfer of information between the ATM and the LAN.

This section of STONER et al. does not explain why incorporating a lower layer processing portion and a higher layer processing portion accessing a same memory space

of a shared memory through physically different memory buses into the LO et al. system would result in dedicated access to components.

For at least the foregoing reasons, Applicants submit that claim 14 is patentable over LO et al., YOKOYAMA et al., and STONER et al., whether taken alone or in any reasonable combination.

Independent claims 15, 16, 18-21, 23, 25-27, and 29 recite features similar to (yet possibly of different scope than) features described above with respect to claim 14. Therefore, these claims are patentable over LO et al., YOKOYAMA et al., and STONER et al., whether taken alone or in any reasonable combination, for at least reasons similar to reasons given above with respect to claim 14.

Claim 17 depends from claim 16. Therefore, this claim is patentable over LO et al., YOKOYAMA et al., and STONER et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 16.

Claim 22 depends from claim 21. Therefore, this claim is patentable over LO et al., YOKOYAMA et al., and STONER et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 21.

Claim 28 depends from claim 27. Therefore, this claim is patentable over LO et al., YOKOYAMA et al., and STONER et al., whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 27.

Claims 24 and 32-34 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over LO et al. in view of YOKOYAMA et al., and further in view of STONER et al. and ALBAL et al. Applicants respectfully traverse this rejection.

Independent claim 24 is directed to a packet processing method for exchanging packet data through a plurality of layers recommended by Open System Interconnection reference model. The method includes storing the entire packet into a packet memory; and storing part of each packet of the packet data used in processes of a layer 2 processing portion and a layer 3 processing portion into a multi-port shared memory, where the layer 2 processing portion and the layer 3 processing portion access the same memory space of the multi-port shared memory. A pipeline processing system is used so that the layer 2 processing portion and the layer 3 processing portion access the shared memory without interference. LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. do not disclose or suggest this combination of features.

For example, LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al., whether taken alone or in any reasonable combination, do not disclose or suggest a pipeline processing system that is used so that a layer 2 processing portion and a layer 3 processing portion can access the shared memory without interference. The Examiner admits that LO et al. and YOKOYAMA et al. do not disclose this feature and relies on elements 9, 11, 13, and 15, in Fig. 1 of STONER et al. for disclosing "separate component buses for pipeline processing" (Office Action, pp. 3-4 and 6). Applicants respectfully disagree with the Examiner's interpretation of STONER et al.

STONER et al.'s Fig. 1 depicts a switch module 1 that includes an ATM interface means 17, LAN interface means 19, and a packet memory 7 connected to a packet switching processor 21 and a management processor 23. In STONER et al.'s Fig. 1, elements 9, 11, 13, and 15 correspond to port means of packet memory means 7 that can

separately read and write information from and to packet memory means 7 (col. 4, lines 11-14). STONER et al. does not disclose or suggest that one of these ports 9, 11, 13, and 15 are part of a pipeline processing system that is used so that a layer 2 processing portion and a layer 3 processing portion can access the shared memory without interference, as required by claim 24. Also, Applicants submit that one skilled in the art would not construe ports 9, 11, 13, and 15, which is part of packet memory means 7, as corresponding to a layer 2 processing portion and a layer 3 processing portion.

Even assuming, for the sake of argument, that that the above portion of STONER et al. could reasonably be construed to disclose a pipeline processing system that is used so that a layer 2 processing portion and a layer 3 processing portion can access the shared memory without interference, Applicants submit that one skilled in the art at the time of Applicants' invention would not have been motivated to incorporate this alleged teaching of STONER et al. into the LO et al. system, absent impermissible hindsight. With respect to motivation, the Examiner alleges "it would have been obvious to one skilled in the art ... in order to give dedicated access between the components" and points to col. 4, lines 11-14 and 43-54, of STONER et al. for support (Office Action, pg. 4). The Examiner's motivation is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation has consistently been held to be insufficient for establishing a *prima facie* case of obviousness. Applicants submit that the Examiner's motivation is based on impermissible hindsight.

Col. 4, lines 11-14, of STONER et al. has been reproduced above. This section of STONER et al. does not explain why incorporating a pipeline processing system that is

used so that a layer 2 processing portion and a layer 3 processing portion can access the shared memory without interference into the LO et al. system would result in dedicated access to components. Instead, this section of STONER et al. merely discloses that memory means 7 include ports 9, 11, 13, and 15 that can separately read and write information from and to memory means 7.

Col. 4, lines 43-54, of STONER et al. is reproduced above. This section of STONER et al. does not explain why incorporating a pipeline processing system that is used so that a layer 2 processing portion and a layer 3 processing portion can access the shared memory without interference into the LO et al. system would result in dedicated access to components.

An important concept that should be noted is that in order to reach a proper determination under 35 U.S.C. § 103, the Examiner must step backward in time and into the shoes of a hypothetical "person of ordinary skill in the art" at a time when Applicants' invention was unknown and just before it was made. With this concept in mind, it appears that the Examiner believes that is conceivable that, having the LO et al. document that is drawn to a system that transfers data between an IEEE 1394 communications domain and an Ethernet communications domain, one skilled in the art at the time Applicants' invention was made, having no knowledge of Applicants' invention, would have combined the LO et al. document with the YOKOYAMA et al. document, drawn to a system that interfaces computers systems utilizing separate paths for control information and data (title), the STONER et al. document, drawn to an ATM/LAN switch module (Abstract), and the ALBAL et al. document, drawn to a

system for handling the D Channel out-of-band signaling protocol of an Integrated Services Digital Network (col. 1, lines 7-10), to come up with Applicants' invention. Irrespective of the fact that these documents are drawn to non-analogous inventions, Applicants submit that one skilled in the art at the time of Applicants' invention would not have been motivated, absent impermissible hindsight, to combine these non-analogous inventions in the manner suggested by the Examiner.

For at least the foregoing reasons, Applicants submit that claim 24 is patentable over LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al., whether taken alone or in any reasonable combination.

Independent claim 32 is directed to a packet exchange for exchanging packet data through a plurality of layers recommended by Open System Interconnection reference model. The packet exchange includes a packet memory for storing the entire packet; a multi-port shared memory for storing part of each packet of the packet data used in processes of a layer 2 processing portion as a data link layer and a layer 3 processing portion as a network layer of the plurality of layers, the layer 2 processing portion and the layer 3 processing portion accessing the same memory space of said multi-port shared memory; and a processor, connected to the layer 2 processing portion and the layer 3 processing portion, for executing a process of a layer higher than layer 3. LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. do not disclose or suggest a processor, connected to the layer 2 processing portion and the

layer 3 processing portion, for executing a process of a layer higher than layer 3. The Examiner does not address this feature in the Office Action. Therefore, a *prima facie* case of obviousness has not been established with respect to claim 32.

Moreover, Applicants' arguments regarding combining LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. are equally applicable to claim 32. Applicants' submit that one skilled in the art at the time of Applicants' invention would not have been motivated to combine LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. in the manner suggested by the Examiner, absent impermissible hindsight.

For at least the foregoing reasons, Applicants submit that claim 32 is patentable over LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al., whether taken alone or in any reasonable combination.

Independent claim 33 is directed to a packet processing apparatus for exchanging packet data through a plurality of layers. The packet processing apparatus includes a packet memory for storing the entire packet; a shared memory as a multi-port memory for storing part of each packet of the packet data used in processes of a layer 2 processing portion as a data link layer and a layer 3 processing portion as a network layer, the layer 2 processing portion and the layer 3 processing portion accessing the same memory space of the shared memory, wherein the layer 2 and 3 are recommended by Open System Interconnection reference model; and a layer 2 reception processing portion for storing only a field necessary for layer 3 or a higher layer to the packet memory and the shared memory. LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination

of features.

For example, LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. do not disclose or suggest layer 2 reception processing portion for storing only a field necessary for layer 3 or a higher layer to the packet memory and the shared memory. The Examiner does not address this feature in the Office Action. Therefore, a *prima facie* case of obviousness has not been established with respect to claim 33.

Moreover, Applicants' arguments regarding combining LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. are equally applicable to claim 33. Applicants' submit that one skilled in the art at the time of Applicants' invention would not have been motivated to combine LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. in the manner suggested by the Examiner, absent impermissible hindsight.

For at least the foregoing reasons, Applicants submit that claim 33 is patentable over LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al., whether taken alone or in any reasonable combination.

Independent claim 34 is directed to a packet processing apparatus for converting packet data through a plurality of layers. The packet processing apparatus includes a packet memory for storing the entire packet; a shared memory for storing part of each packet of the packet data used in processes of a lower layer processing portion and a higher layer processing portion, the lower layer processing portion and the higher layer processing portion accessing the same memory space of the shared memory through physically different memory buses; and a layer 2 transmission processing portion for combining data stored in a plurality of packet memories and data stored in said shared

memory and transmitting the resultant data as the packet, wherein the layer 2 is recommended by Open System Interconnection reference model. LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

For example, LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. do not disclose or suggest the lower layer processing portion and the higher layer processing portion accessing the same memory space of the shared memory through physically different memory buses. The Examiner admits that LO et al. and YOKOYAMA et al. do not disclose this feature and relies on elements 9, 11, 13, and 15, in Fig. 1 of STONER et al. for disclosing "separate component buses for pipeline processing" (Office Action, pp. 3-4). Applicants respectfully disagree with the Examiner's interpretation of STONER et al.

STONER et al.'s Fig. 1 depicts a switch module 1 that includes an ATM interface means 17, LAN interface means 19, and a packet memory 7 connected to a packet switching processor 21 and a management processor 23. In STONER et al.'s Fig. 1, elements 9, 11, 13, and 15 correspond to port means of packet memory means 7 that can separately read and write information from and to packet memory means 7 (col. 4, lines 11-14). STONER et al. does not disclose or suggest that one of these ports 9, 11, 13, and 15 can access a same memory space of packet memory means 7 through physically different memory buses, as required by claim 34. Also, Applicants submit that one skilled in the art would not construe ports 9, 11, 13, and 15, which is part of packet

memory means 7, as corresponding to a lower layer processing portion and a higher layer processing portion.

Even assuming, for the sake of argument, that that the above portion of STONER et al. could reasonably be construed to disclose a lower layer processing portion and a higher layer processing portion accessing a same memory space of a shared memory through physically different memory buses, Applicants submit that one skilled in the art at the time of Applicants' invention would not have been motivated to incorporate this alleged teaching of STONER et al. into the LO et al. system, absent impermissible hindsight. With respect to motivation, the Examiner alleges "it would have been obvious to one skilled in the art ... in order to give dedicated access between the components" and points to col. 4, lines 11-14 and 43-54, of STONER et al. for support (Office Action, pg. 4). The Examiner's motivation is merely a conclusory statement regarding an alleged benefit of the combination. Such motivation has consistently been held to be insufficient for establishing a *prima facie* case of obviousness. Applicants submit that the Examiner's motivation is based on impermissible hindsight.

Col. 4, lines 11-14, of STONER et al. is reproduced above. This section of STONER et al. does not explain why incorporating a lower layer processing portion and a higher layer processing portion accessing a same memory space of a shared memory through physically different memory buses into the LO et al. system would result in dedicated access to components. Instead, this section of STONER et al. merely discloses that memory means 7 include ports 9, 11, 13, and 15 that can separately read and write information from and to memory means 7.

Col. 4, lines 43-54, of STONER et al. is reproduced above. This section of STONER et al. does not explain why incorporating a lower layer processing portion and a higher layer processing portion accessing a same memory space of a shared memory through physically different memory buses into the LO et al. system would result in dedicated access to components.

LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. do not further disclose or suggest a layer 2 transmission processing portion for combining data stored in a plurality of packet memories and data stored in said shared memory and transmitting the resultant data as the packet, as also required by claim 34. The Examiner does not address this feature in the Office Action. Therefore, a *prima facie* case of obviousness has not been established with respect to claim 34.

Moreover, Applicants' arguments regarding combining LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. are equally applicable to claim 34. Applicants' submit that one skilled in the art at the time of Applicants' invention would not have been motivated to combine LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al. in the manner suggested by the Examiner, absent impermissible hindsight.

For at least the foregoing reasons, Applicants submit that claim 34 is patentable over LO et al., YOKOYAMA et al., STONER et al., and ALBAL et al., whether taken alone or in any reasonable combination.

Claim 30 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over LO et al., in view of YOKOYAMA et al., and further in view of HIGUCHI et al. Applicants respectfully traverse this rejection.

Independent claim 30 is directed to a packet exchange for exchanging packet data through a plurality of layers recommended by Open System Interconnection reference model. The packet exchange includes a layer 2 reception processing portion for receiving a packet, storing the received packet to a packet memory, and storing a header portion of the received packet into a shared memory; a layer 3 processing portion for receiving the header portion, executing a network process corresponding to the header portion, updating the header portion when necessary, and storing the updated header portion into the same address of said shared memory; and a layer 2 transmission processing portion for combining the updated header portion received from said layer 3 processing portion and stored in the shared memory and packet information stored in the packet memory and transmitting the resultant data as a packet. The layer 2 transmission processing portion combines data updated by the layer 3 processing portion and stored in the shared memory and packet data stored in the packet memory, transmits the combined data, converts a packet format into a format of layer 1, and when layer 3 is an IP (Internet Protocol) layer, converts an IP V4 (Version 4) packet into an IP V6 (Version 6) packet or vice versa. LO et al., YOKOYAMA et al., and HIGUCHI et al. do not disclose or suggest this combination of features.

The Examiner does not address the specific features recited in claim 30. Instead, the Examiner relies on LO et al. for allegedly disclosing "a packet processing apparatus (fig. 4) for converting packet data through several layers (fig. 5, item 520 and 525; col. 8, lines 35-43). The apparatus comprises a packet memory for storing a user information portion of a packet data (abstract, lines 5-13; fig. 7, step 710). The apparatus combines a

new header portion with a user information portion stored in a packet memory as a packet to be transmitted (col. 9, lines 10-13 and 35-40). The lower layer portion is layer 2 and the higher layer portion is layer 3 (fig. 5, step 252; note: MAC at layer 2 and IP at layer 3 of an OSI reference model)," on YOKOYAMA et al. for allegedly disclosing "a packet processing apparatus (fig. 8) comprising a shared memory (item 30) for storing in a same memory space part of each of the packet data accessed by the layer 2 and layer 3 processing (fig. 10; col. 6, line 61 through col. 7, line 2). A header portion (fig. 7) in the shared memory data is written at the time of packet reception and read at the time of packet transmission by a lower level layer (fig. 13, step 1034; fig. 12, item 1014-1016), and for processing by a higher level layer (fig. 14, step 1037-1038). The same memory space is accessed by the layer 2 and layer 3 processes (col. 7, lines 41-42; fig. 10; item E3; fig. 12, steps 1011-1012 and 1014; fig. 13, step 1034; fig. 14, step 1037) and a layer 1 format packet is created (fig. 3, physical; fig. 2, item 40; fig. 8, item 22-4)," and on HIGUCHI et al. for allegedly disclosing "a layer 2 process (fig. 2, item 1006) for converting between IPv4 and IPv6" (Office Action, pp. 4-5). Even assuming, for the sake of argument, that the sections of LO et al., YOKOYAMA et al., and HIGUCHI et al. disclose what the Examiner alleges that they disclose (a point that Applicants do not concede), Applicants submit that these allegations by the Examiner in no way address the specific features recited in Applicants' claim 30. The Examiner has not established a *prima facie* case of obviousness with respect to claim 30. If this rejection is maintained, Applicants respectfully request that the Examiner specifically address the features of claim 30.

For at least the foregoing reasons, Applicants submit that claim 30 is patentable over LO et al., YOKOYAMA et al., and HIGUCHI et al., whether taken alone or in any reasonable combination.

Claim 31 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over LO et al. in view of YOKOYAMA et al., and further in view of HIGUCHI et al. and TSUCHIYA et al. Applicants respectfully traverse this rejection.

Independent claim 31 is directed to a packet exchange for exchanging packet data through a plurality of layers recommended by Open System Interconnection reference model. The packet exchange includes a layer 2 reception processing portion for receiving a packet, storing the received packet to a packet memory, and storing a header portion of the received packet into a shared memory; a layer 3 processing portion for receiving the header portion, executing a network process corresponding to the header portion, updating the header portion when necessary, and storing the updated header portion into the same address of the shared memory; and a layer 2 transmission processing portion for combining the updated header portion received from said layer 3 processing portion and stored in the shared memory and packet information stored in the packet memory and transmitting the resultant data as a packet. The layer 2 transmission processing portion combines data updated by the layer 3 processing portion and stored in the shared memory and packet data stored in the packet memory by the layer 2 reception processing portion, and when layer 3 is an IP (Internet Protocol) layer, performs an IP V6 tunneling process for an IP V4 packet, an IP V4 tunneling process for an IP V6 packet, or an IP V4 tunneling process for an IP V4 packet. LO et al., YOKOYAMA et al., HIGUCHI et al.,

and TSUCHIYA et al., whether taken alone or in any reasonable combination, do not disclose or suggest this combination of features.

The Examiner does not address the features recited in claim 31. Instead, the Examiner relies on the rejection of claim 30. As set forth above, the Examiner does not address the features recited in claim 30. The arguments set forth above with respect to claim 30 are equally applicable here. The Examiner has not established a *prima facie* case of obviousness with respect to claim 31.

The Examiner relies on col. 2, lines 1-16, of TSUCHIYA et al. for allegedly disclosing "IP tunneling" (Office Action, pg. 5). Applicants note that claim 31 does not merely recite IP tunneling. Instead, claim 31 specifically recites a layer 2 transmission processing portion performs, when layer 3 is an IP (Internet Protocol) layer, an IP V6 tunneling process for an IP V4 packet, an IP V4 tunneling process for an IP V6 packet, or an IP V4 tunneling process for an IP V4 packet. The Examiner has not addressed these features.

At col. 2, lines 1-16, TSUCHIYA et al. discloses:

> IETF also proposed a method called an IP tunneling. This is a method such that when the IPv4 network exists on a communication path between two IPv6 terminals and a communication cannot be executed directly by the IPv6 packet, the IPv6 packet is encapsulated by the IPv4 header and is allowed to pass through the IPv4 network. Similarly, when the IPv6 network exists on a communication path between the IPv4 terminals and a communication cannot be executed directly by the IPv4 packet, the IPv4 packet is encapsulated by the IPv6 header and is allowed to pass through the IPv6 network. Consequently, even when there is the IPv4 network on the communication path, the communication between the IPv6 terminals can be executed. Even when there is the IPv6 network on the communication path, the communication between the IPv4 terminals can be executed.

This section of TSUCHIYA et al. discloses encapsulating an IPv6 packet by an IPv4 header to allow the IPv6 packet to pass through an IPv4 network and encapsulating an IPv4 packet by an IPv6 header to allow the IPv4 packet to pass through an IPv6 network. This section of TSUCHIYA et al. does not disclose or suggest a layer 2 transmission processing portion that performs, when layer 3 is an IP layer, an IP V6 tunneling process for an IP V4 packet, an IP V4 tunneling process for an IP V6 packet, or an IP V4 tunneling process for an IP V4 packet, as required by claim 31.

Even assuming, for the sake of argument, that the above section of TSUCHIYA et al. could reasonably be construed to disclose the above features of claim 31, Applicants submit that one skilled in the art at the time of Applicants' invention would not have been motivated to combine this alleged teaching of TSUCHIYA et al. with LO et al., absent impermissible hindsight. With respect to motivation, the Examiner alleges "it would have been obvious to one skilled in the art ... to have IP tunneling in the invention of Lo in view of Yokoyama and Higuchi in other to transmit an IP packet to a destination device" (Office Action, pg. 5). Applicants submit that the Examiner's motivation is merely a conclusory statement regarding an alleged benefit and is insufficient for establishing a *prima facie* case of obviousness. Moreover, the Examiner's motivation seems to indicate that the system of LO et al. is incapable of transmitting an IP packet to a destination. Applicants direct the Examiner's attention to Fig. 5 of LO et al. that specifically discloses transferring a data packet from a first communication domain to a second communication domain. Thus, Applicants submit that LO et al. already discloses the ability to transmit an IP packet. The Examiner's motivation for combining LO et al.,

YOKOYAMA et al., HIGUCHI et al., and TSUCHIYA et al. is impermissibly based on hindsight.

For at least the foregoing reasons, Applicants submit that claim 31 is patentable over LO et al., YOKOYAMA et al., HIGUCHI et al., and TSUCHIYA et al., whether taken alone or in any reasonable combination.

In view of the foregoing amendments and remarks, Applicants respectfully request the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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